IN THE CLAIMS:

Please cancel claims 22 and 26-28 without prejudice.

Please amend claims 1-3, 5, 6, 11, and 23-25, and add new claim 29 as follows:

1. (Currently Amended) An adjustable harmonic distortion detector comprising:

a clock signal source;

means for detecting a first period of evaluation;

means for detecting a second period of evaluation;

a first block for ~~memorizing~~ storing a number equal to the clock pulses present in the first period of evaluation;

a multiplier block for performing a multiplication between the number stored in the first block and a multiplicative factor during the second period of evaluation; and

a second block for ~~memorizing~~ storing the outcome of the multiplication, the second block adapted to generate an output signal when the ~~outcome~~ value stored in the second block is equal to zero.

2. (Currently Amended) The distortion detector according to the claim 1, wherein the multiplicative factor is a ~~predetermined~~ fixed number.

3. (Currently Amended) The distortion detector according to the claim 1, wherein the multiplicative factor is a function of the number of clock signal pulses stored in the first block.

4. (Original) The distortion detector according to the claim 1, wherein the multiplicative factor is deduced from the correlation between the ratio of the second and first period of evaluation and the total distortion value according to a diagram.

5. (Currently Amended) The distortion detector according to the claim 1,

wherein the first block receives in input the clock signal, and the first evaluation period,

the multiplier block receives at input the clock signal, the multiplicative factor, and the output signal of the first block, and

the second block receives at input the clock signal, the output signal of the multiplier block, and the second evaluation period, and produces an output signal during the simultaneous combination of the clock signal and the second evaluation period.

6. (Currently Amended) The distortion detector according to the claim 1,

wherein the first block receives at input the clock signal, and the first evaluation period,

the multiplier block receives at input the clock signal, the second evaluation period, and a signal generated by a fourth block adapted to realize a correspondence function between the number of clock pulses ~~counted~~ stored in ~~the measure period of~~ the first block and the diagram, and

the second block receives at input the clock signal, the output signal of the multiplier block, and the second evaluation period, and ~~it~~ produces an output signal during the second evaluation period.

7. (Original) The distortion detector according to claim 1, wherein the first evaluation period provides the length from the crossing of the abscissa axis to the start of the distortion step of the output signals.

8. (Original) The distortion detector according to claim 7, wherein the second evaluation period provides the length from the start of the distortion step to the end of the same of the output signals.

9. (Previously Presented) The distortion detector according to claim 1, wherein the first block is an up counter.

10. (Original) The distortion detector according to claim 9, wherein the second block is a down counter.

11. (Currently Amended) The distortion detector according to claim 10, wherein a fourth block is coupled to an input of the multiplier block, the fourth block ~~makes~~ making the correspondence function between the number of clock pulses ~~counted in the first evaluation period and~~ stored in the first block and the diagram.

12-22. (Canceled)

23. (Currently Amended) A method for detecting harmonic distortion, said method comprising the steps of:

counting a number of clock signal pulses in a first period of evaluation;

~~inserting~~ storing the number in a first block;

~~inserting a multiplicative factor in a second block;~~

multiplying the ~~value~~ number stored in the first block with ~~the value stored in the second block~~ a multiplicative factor during a second period of evaluation;

decreasing the outcome of the multiplying step during the second period of evaluation;

generating a signal in the case that the outcome of the deceasing step is zero.

24. (Currently Amended) The method according to the claim 23, wherein the multiplicative factor is a ~~predetermined~~ fixed number.

25. (Currently Amended) The method according to the claim 23, wherein the multiplicative factor is a ~~value in~~ function of the ~~pulse~~ number stored in the first block.

26-28. (Canceled)

29. (New) The distortion detector according to claim 1, wherein, during the second period of evaluation, the second block decreases the value stored in the second block, and generates the output signal when the value stored in the second block reaches zero.